Modeling Techniques for Board Level Drop Test for a Wafer-Level Package

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Abstract

Reliability performance during drop impact is critical for electronic handheld devices. In this paper, a comprehensive study in efficiency and accuracy of multiple finite element modeling approaches and solution techniques for a wafer-level package (WLP) is presented. JEDEC specified test board is used for the model study. A direct acceleration input method is introduced. Two types of global finite element models for a typical WLP are studied: solder layer and solder bump models. Two different approaches, full implicit dynamics and mode superposition, are applied to solve the JEDEC board dynamic responses. Based on this study, the 8-node solid element with smeared solder layer model, and the full implicit dynamics with either input-G or direct acceleration method are recommend. This combination results in short solution time and produces accurate dynamic solutions for drop test board. It has been found that the fundamental natural frequency of a JEDEC board with WLP typically ranges from 200 to 250 Hz for a large range of array size. There is a large strain gradient close to the component edge for each package on the test board. Due to the rigidity of the silicon chip, the board strain at the center of each component on the opposite side of PCB does not reflect the local bending behaviors of the board. The center of the board between two components might be a stationary point, which does not capture the board bending. With the increase of the chip size, the board strain at edge of each component will increase. The board peak strain at the corner package (U1, U5, U11, and U15) has been found greater than that at the center package (U8), but the bending direction is opposite. The components U6 and U10 have lowest board strains among all components.

1. Introduction

Reliability of handheld electronic devices such as cell phones and PDAs due to drop/impact event is a major concern in electronics industry. During a drop/impact event, the PCB assembly inside the phone casing vibrates causing a flexural/bending motion of the board. The PCB bending results in high stress or strain on solder joints of electronic components due to high level of impact forces. It ultimately leads to the failure in solder joints. The failure can occur at package side or PCB side. Other failure modes such as pad-crater and broken board traces are also observed.

A number of excellent papers have been written on drop characterization and simulations [2-7]. Finite element modeling using commercial software such as ANSYS and ABAQUS have been used extensively for the simulation of drop impact test, and have been successfully applied in product developments [8-9]. Attempts have been made to improve the methodology for simulation and to reduce the computational time [9-10]. The input-G method exerts to the mounting hole location the acceleration impulse measured in experiment. This decouples the board finite element model from the system model. Therefore, the computational efficiency has been significantly improved. An alternative method is the input-D method [11-12]. With this method, the acceleration input is converted to the displacement input through integration over time. There are several approaches in implementing the input-G method. Tee et al. [4] uses explicit dynamics analysis by directly applying acceleration impulse in DYNA-3D. The implicit dynamics method can also be used to solve board dynamic response. For this method however, surface acceleration load is not supported. To get around this difficulty, Syed et al [9] proposed to convert acceleration input into force input by multiplying the acceleration with the large mass. This large mass method with rigid elements effectively applies the acceleration on the support points. The mode superposition method [13] requires shorter computational time than both explicit and implicit methods.

This paper presents a comprehensive study to investigate the efficiency and accuracy of different models and approaches for PCB global dynamic response. A WLP is used for this study. Two kinds of global finite element models for a typical WLP solder ball array are studied: solder layer and solder bump models. Two different solution approaches for JEDEC board dynamic response are compared against each other: full implicit dynamics and mode superposition. For the acceleration input, this paper introduces a direct acceleration input method [14]. The results are compared to the input-G method. Finally, the effect of different parameters such as chip size, acceleration magnitude, and board strain distributions are studied. The effect of boundary conditions on the structure is also taken into account here.

2. JEDEC Board Drop Impact Test

JEDEC drop test standard JESD22-B111 [1] is commonly used for board level drop test for many years. JESD22-B111 recommends 15 components mounted on the PCB in 3 rows of 5 components each. The PCB is mounted on a base plate with 4 mounting screws at the corners. This base plate is then mounted on a drop table. The drop table, guided by guide rods, is allowed to strike on a rigid base from some specified height. A half sine-impulse is produced when the table strikes the rigid base. A layer of felt is used on the strike surface to obtain the desired load conditions. Finite element method is often used to calculate the dynamic response of the drop test board and to correlate the drop impact performance.

It is difficult to include all involved parts in the finite element model. The size of the finite element model will be

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very large if all details of drop table, PCB, and all components on PCB are included. In this case the numerical difficulties will be encountered to deal with the contact simulation between the felt and drop table block. Since the main interest is focused on the failures of tiny solder balls of each component, the dimension ratio from the table block to the solder ball IMC layer will be too large to handle. In order to reduce the computational time, the Input-G method can be applied to decouple the board dynamic responses from the test system by applying the 'Table-G' directly to the board. This avoids the difficulties in modeling the complex behaviors of contact between the drop table and drop surfaces.

3. Simulation Methodology

To understand the behavior of a structure during drop impact test we will consider mainly two simulation methods used in standard ANSYS (without explicit dynamics solver). The first method is Full Implicit Dynamics which uses the full system matrices to calculate the transient response (no matrix reduction). The second method is called Mode-superposition method. This method sums factored mode shapes (eigenvectors) from a modal analysis to calculate the structure's response. There are pros and cons for both methods. On one hand, the full method allows material and geometric nonlinearities while mode-superposition method considers linear problem only. On the other hand, mode-superposition method in general is faster (theoretically) and less expensive compared to the full method.

To produce the desired G input loading (1500G, 0.5 milliseconds duration, half-sine pulse), we consider two different approaches for each of the above methods here. These two approaches are referred to as Input G with Large Mass method and Direct Input Acceleration method. In input G method, a large mass element is attached to the nodes around the screw holes using rigid elements. The acceleration input is converted into force input by multiplying the acceleration with large mass. This large mass method with rigid elements effectively applies the acceleration on the support points. With direct input acceleration method, on the other hand, half-sine impulse load is directly applied to the model as inertia body force. With this input, the screw hole boundary conditions must be specified.

Some of the main challenges involved in finite element modeling for JEDEC board dynamic responses are:

- Very large finite element models with various mesh densities to transform from millimeter scale to micron scale within one model.
- The level of mesh density also impacts the solution time not only because of model size but also due to time step size requirements during dynamic simulation.

In order to minimize the difficulties involved in modeling and to reduce computational time, two finite element models are built here. The first finite element model is Solder Bump model. In this model the shape of the solder bump is simplified to a rectangular block as shown in figure 1. The complete model consists of a PCB, rectangular solder bumps and chips. A quarter 3D-model is built due to symmetry (figure 1). The size of the chip and number of solder arrays can be varied for the experiments. The second model built is Solder Layer model. The model smears individual solder bumps into a uniform layer with effective material properties. Such a model can reduce the board model size significantly since the size of finite element model does not depend on the numbers of solder bumps, as shown in Figure 2. 3-D solid elements are used for PCB, silicon chip and solder layer or bumps, which is different from the global model in Syed's paper where the shell element is used for PCB. Since the mesh has been optimized, both models run very effectively with a regular PC by implicit dynamics. For a 6x6 mm chip size the solder bump model has 13161 elements compared to 5569 for the solder layer model. The computational time taken by solder layer model is reduced to 1/3 of that solder bump model. Table 1 lists the material properties used in this paper.

Table1. Material properties

Materials	Modulus (MPa)	Poisson Ratio	Density x 10^{-3} (gm/mm^3)
PCB	22000	0.25	2.1
Solder bumps	51000	0.36	7.2
Chip	130000	0.278	2.5

4. Model Study

In this section, WLP solder ball models, PCB dynamic response solution method, and input acceleration load application options are studied. The test model used for this case and for all the following cases is a 6x6 mm chip size model.

4.1Comparison between Two Models (Solder Layer vs. Solder Bump)

Two solder ball models and two PCB dynamic response solution methods are examined. Modal analysis is discussed first.

4.1(a) Modal Analysis

Modal analysis is used to determine the natural frequencies and mode shapes of a structure. The natural frequencies and mode shapes are then used to obtain the transient response by superposition.

The nature frequencies for the drop test board are listed in Table 2. The solder balls are modeled two ways, solder bump model (individual cubic blocks), and solder layer model (a homogeneous layer). It is seen from the Table 1 that the lowest five natural frequencies obtained by both solder ball models solder layer are approximately the same. This suggests that solder layer may be used in the drop test simulations without sacrificing the accuracy.

Table 2. Modal analysis of the two models

Mode No.	Frequency (Hz)		Difference
	Model A Solder Bump	Model B Solder Layer	
1	212	210	0.9%
2	551	548	0.3%
3	915	913	0.2%
4	1257	1251	0.4%
5	2193	2181	0.5%

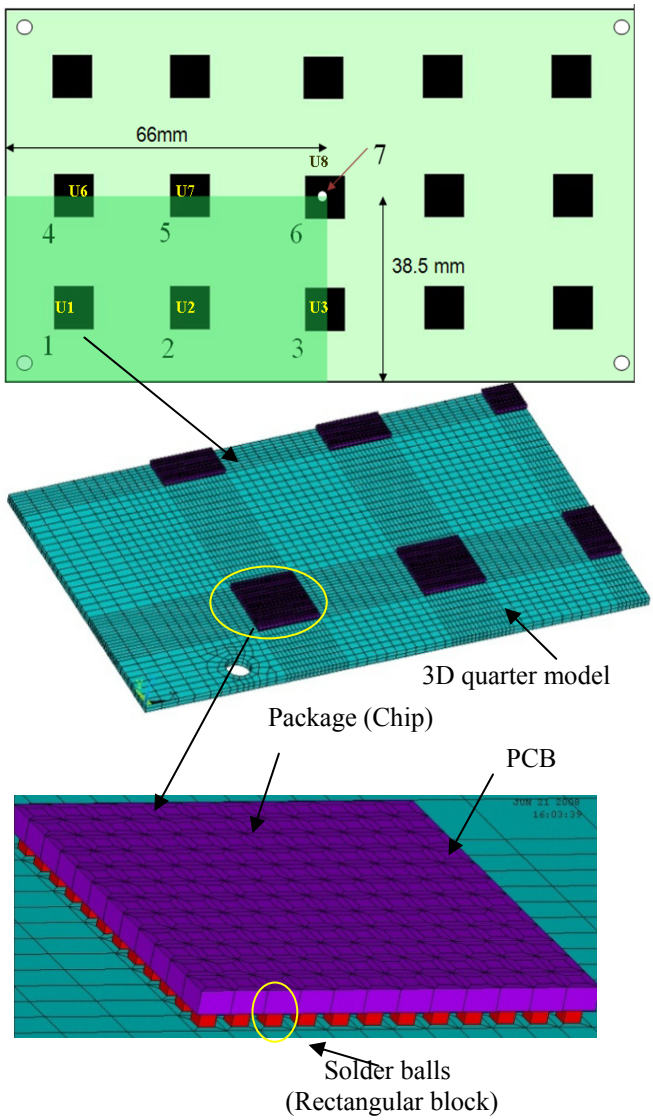


Figure 1. 3D-quarter model of JEDEC board (Solder bump model)

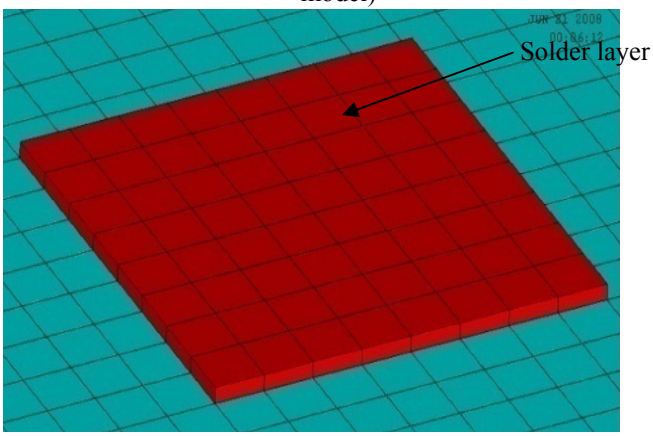


Figure 2 Details at Solder Layer model

4.1(b) Transient Dynamic Analysis

The two solder ball models are then solved with input G method with full implicit dynamics. The acceleration at site 7 for first 7ms during the impact is plotted in Figure 3. Site 7 is at the top of the center component. (Figure 1). It is seen from Figure 3 that the difference between the dynamic response obtained for two models at site 7 is trivial.

The board strain along path 1-3 in Figure 1 is used to examine strain solutions by different approaches. The normal strain in x-direction ε_x at t=1.5 ms is plotted in Figure 4. It is seen that the strain solution for the two solder ball models are almost the same. The difference is mainly at the peaks. This suggests that the solder layer model can be used for board global dynamic response to significantly save computer space and reduce the solution time without sacrificing accuracy.

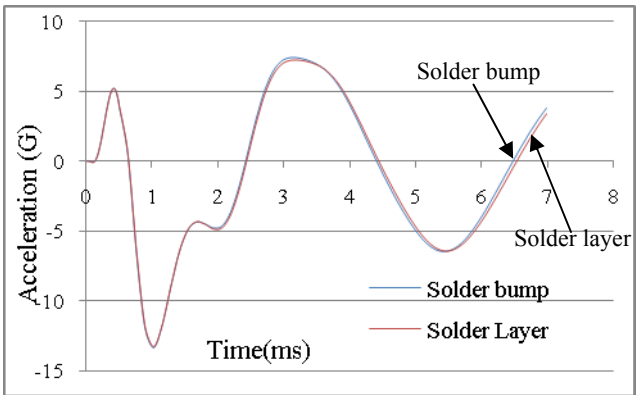


Figure 3. Comparison of acceleration curves for two models (input G method)

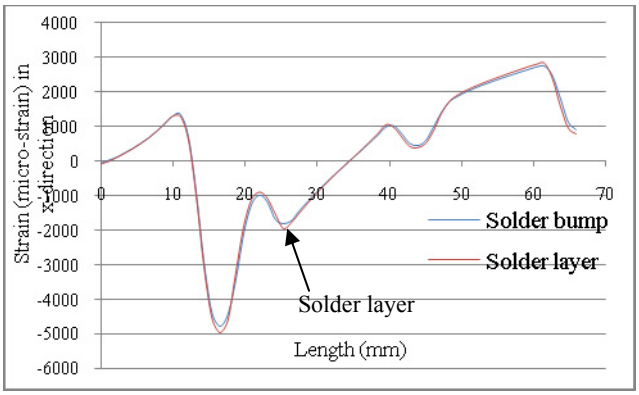


Figure 4. Comparison of board strain for two models

4.2 Comparison of Input G and Direct Input Acceleration Method

Both input G and direct input acceleration are used with a solder bump model. The acceleration history and board strain history results are plotted in Figures 5 to 7. Figure 5 shows the time-dependent acceleration curve at the location 7 (figure 1). It is seen that the acceleration solutions have different values for the initial 0.5 ms acceleration impulse period. However, after this period they overlap. The difference between these two curves is exactly the half-sine acceleration impulse. This suggests that the calculated acceleration from direct acceleration input method includes the initial acceleration applied anywhere in the structure during impact.

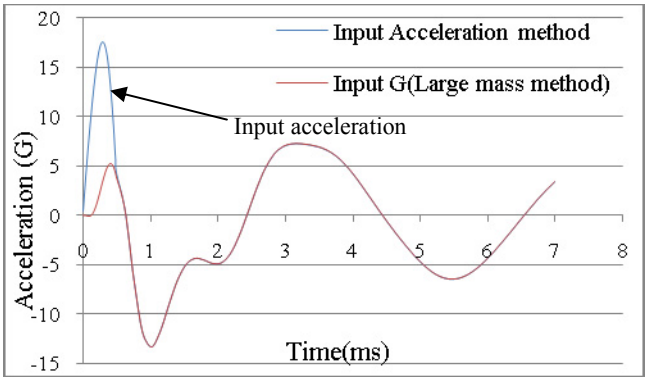


Figure 5. Comparison for input G and input acceleration methods

The board strain along path 1-3 at t=1.5 ms are plotted in Figures 6 and 7. As is seen that the same results are obtained for input G and input acceleration method.

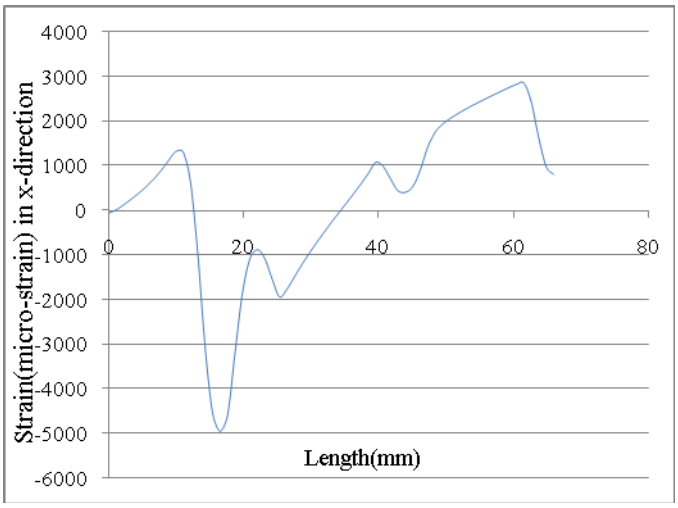


Figure 6. Board strain for input G method (full dynamics)

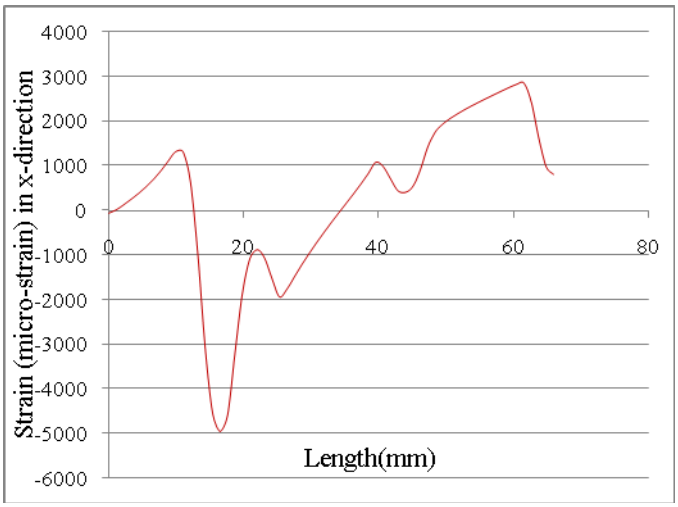


Figure 7. Board strain for input acceleration method (full dynamics)

4.3 Comparison of Full Dynamics and Mode-Superposition Method

The board strains calculated with both full dynamics and mode-superposition methods are is plotted in Figure 8. It is seen that board strains obtained with both solution methods have the same trend. However, peak value of strain is different. It is approximately 5000 micro-strain for full dynamics while it is approximately 4000 micro-strain for mode-superposition method. The board strain and displacement (in z-direction) obtained with the two methods are plotted in figures 9 and 10. It can be seen that solutions with both methods follow the same trends. However, the magnitudes of strain and displacement solutions with these two methods are different. The mode-superposition method always seems to give numerically less value than the full transient analysis.

It is observed from Figures 9 and 10 that the maximum elastic strain occurs near the mounting hole, while the board center has the most deflection. Furthermore, the mounting hole region is bent in the opposite direction compared to the board center.

It should be pointed out here that there are some problems regarding post-processing in ANSYS for the mode-superposition method. The acceleration-time history cannot be plotted. It is sometimes difficult to obtain strain history plots as well. In addition, it takes longer time to post process obtain the full solution by expansion (using EXPASS command). The mode-superposition occupies more memory space than full dynamics. For a case studied, with 6x6mm chip size, mode-superposition method takes more than 4 times the memory space than that of full dynamics. The full dynamics, on the other hand, takes longer time to calculate the full solution. However, it takes overall shorter time since the post processing is fast. Therefore, full dynamics approach is preferred.

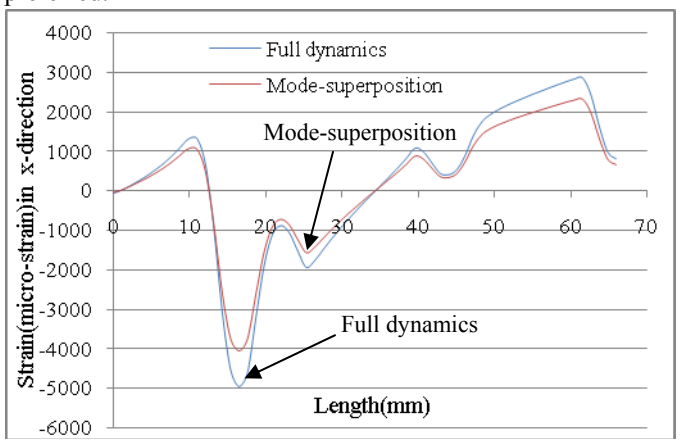
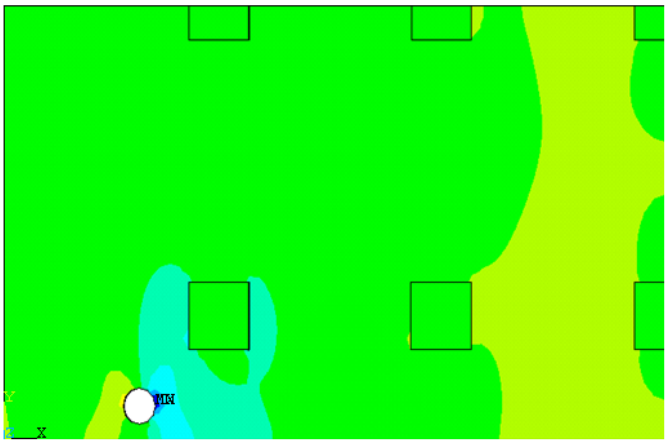


Figure 8. Comparison of board strain full dynamics and mode-superposition method



Board strain in x-direction at time 1.5 ms
Full dynamics analysis method

Mode superposition
method

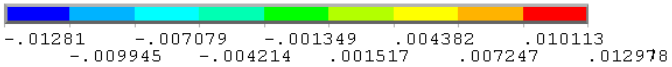
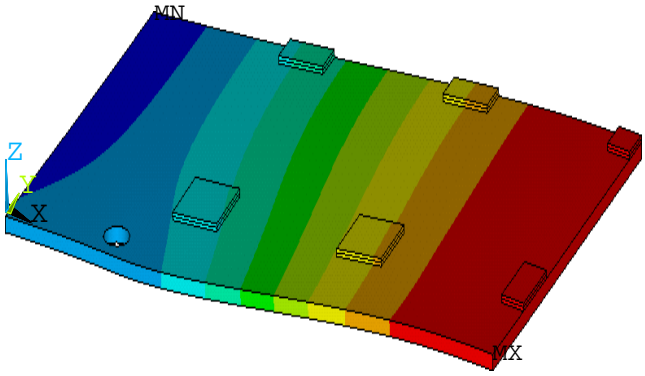


Figure 9. Comparison of board strain for input acceleration and input G

Fig. 11 and 12 plot elastic strain history at location 1 and location 6, respectively for both strains in x- and y- direction. We can see that strain components in x-direction and y-direction at the board corner (1mmx1mm from U1) are much higher than those at board center (1mmx1mm from U8) and bending direction is opposite. Strain in y-direction has higher frequency than the strain in x-direction.



Board displacement in z-direction at time 1.5 ms
Full dynamics analysis method

Mold-superposition Method

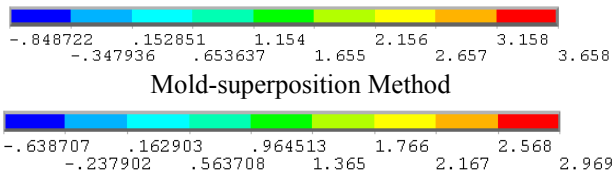


Figure10. Comparison of board displacement (in z-direction) for full dynamics and mode-superposition method

The board displacements in x and y directions for site 1 and 6 (figure 1) are plotted in figures 11 and 12. There are two three observations:

a. the strain in x direction is dominant
b. the strain components in both x and y directions are opposite between locations 1 and 6.
c. Strain component is x direction corresponds to the fundamental natural frequency, and the strain component is y direction corresponds to the 2nd fundamental frequency.

In the following discussion, PDCB strain in x direction ε_x is used to quantify the drop impact performance of WLP. Larger ε_x corresponds to larger PCB bending and worse WLP drop impact performance.

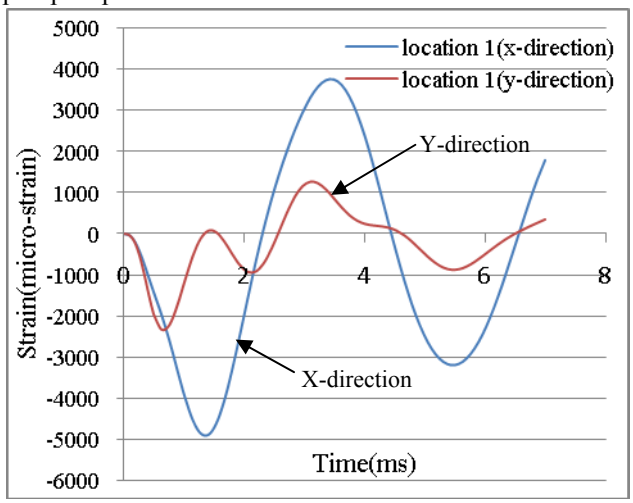


Figure 11. Board strain at location 1

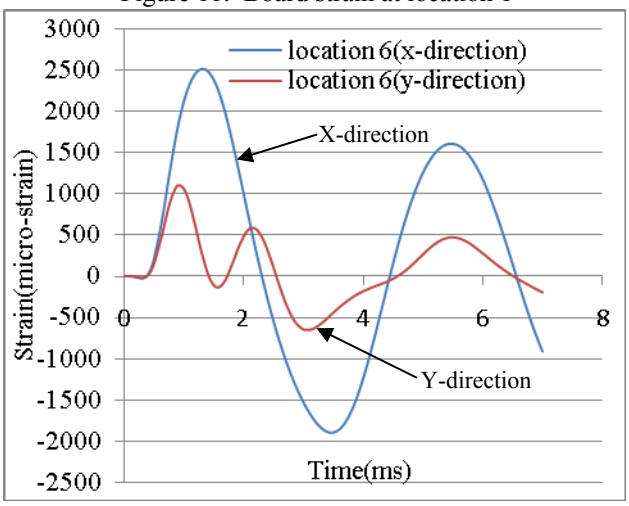


Figure 12. Board strain at location 6

4.4 Comparison of 8 Node vs. 20 Node Finite Element

Two element types, 8 node element (solid 45) and 20 node element (solid 95) may be used for the model. The general expectation is that 20 node element gives more accurate results but the model will take much more computer space and significantly longer time to solve the problem. In order to quantify the effect of element choice comparison is done between the models with these two element types. The results obtained with these two element types are plotted in Figure 13. It is shown that the ε_x difference obtained with 8 node and 20 node elements is trivial (<7%). The results differ mainly at the peaks. Therefore, 8 node element can be used to calculate PCB global dynamics without sacrificing accuracy. The benefit of using 8 node element is significant reduction of computational time. For a typical model, 8 node element

reduces the computational type by 2/3, compared to 20- node element. Such results are observed differently when ABAQUS software is used [15].

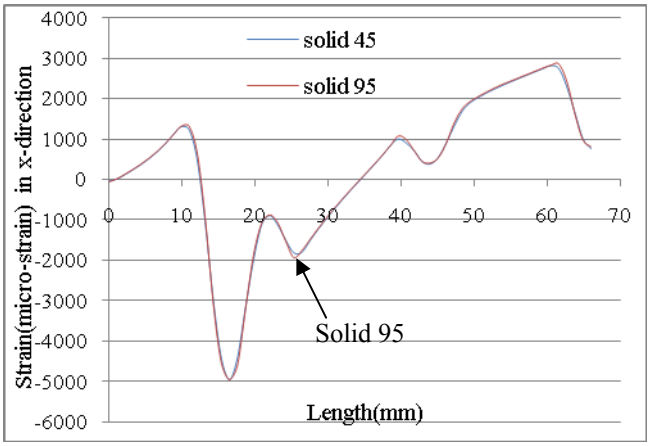


Figure13. Comparison of board strain for 8 node and 20 node elements

5. Results and Discussions

5.1 Effect of the Boundary Condition at Mounting Hole on System Natural Frequency

The boundary conditions at mounting the hole have some effect on the natural frequencies of the system. A 6x6 mm chip size model is studied for this effect. Two types of boundary conditions are considered. The first one is fixing displacement in z-direction only. The second boundary condition is fixing displacement in all directions at mounting hole. The natural frequencies obtained from models with these two different boundary conditions are listed in table 3. It is seen that slightly higher natural frequencies are obtained when displacements of all directions are fixed at mounting hole. This is due to the fact that the board becomes less flexible under this boundary condition. Overall, the fundamental frequency is from 200 to 250 Hz, which is consistent with many test results.

Table 3. Effect of boundary conditions on natural frequency of the model

Mode No.	Natural frequency (Hz)	
	Only Z direction is fixed	All (X,Y,Z) are fixed
1	212	241
2	551	638
3	915	939
4	1257	1338
5	2193	2272

5.2 Effect of Chip Size on System Frequency

To study the effects of chip size on the natural frequency of the system, the chip sizes of 3x3, 4x4, 5x5 and 6x6 mm are considered. The corresponding solder ball arrays are 6x6, 8x8, and 10x10, respectively. For this comparison the displacement in z-direction only is fixed. It is seen in Table 4 that natural frequencies of the system slightly increase with increase in the chip size.

At this point, it is of interest to understand the natural frequency shift. The natural frequency of a system can be expressed by eq. (1). The frequency depends on the stiffness and mass of the system. As the chip size increases the stiffness and mass of the system also increases. In this case however, the board stiffening is dominant leading to increase in the frequency of the system.

$$f := \frac{1}{2\pi}\sqrt{\frac{k}{m}} \qquad \text{eq. (1)}$$

Where k = stiffness of system, N/mm
m = mass of the system, gm

Table 4. Effect of chip size on natural frequency of the model

Mode Number	Natural Frequency (Hz)			
	size (3x3)	size (4x4)	size (5x5)	size (6x6)
1	209.11	209.74	210.59	211.59
2	542.41	544.46	547.24	550.66
3	879.94	887.84	899.59	915.22
4	1234.9	1239.3	1246.4	1256.6
5	2118	2135.8	2161.0	2192.6

5.3 Board Strain Distribution

The board strain in x-direction at 6 different locations is plotted in Figure 14. and following observations are made. The strain location is at points 1, 2, 3, 4, 5 and 6 which are at 1x1 mm away from the their respective package corners at the PCB component side, as defined in Figure 1. Components at center column (U3 and U8), the next column (U2 and U7) are subjected to bending in the same direction. In addition, U3 and U8 are subjected to a larger bending than U2 and U7. However, the outer column components U1 and U6 are subjected to bend in opposite direction. It is important to note that due to the mounting screw effect, the peak board strain at the corner of U1 is greater than that at U8. This obervation is from the results showed in Syed's paper. Figure 15 plots the strain in x-direction at 6 different locations in the center of each component. It is found that chip center strain values are much loert compared to the corner strain. It is also noted that the center strain at U8 is greater than that at U1. From the Figure 14, the peak positive strain values at the corner of the component can be ranked in the order of U1>U3>U8>U2>U7>U6.

It is generally expected that drop test failure is due to the peeling stress at solder joint caused by board bending. The board strain is propotional to the degree of board bending. Since there is significantly different board strain values during the drop, the drop impact life of a given WLP is different for different component locations. Based on results of this study, the drop impact lift of a given WLP can be ranked in therms of component locations: U1<U3<U8<U2<U7<U6. This is in agreement with experimental results.

It is important to review the effectivness of the JEDEC board specification JESD22-B111. The JEDEC drop test is mainly used for relative component performance. However, the drop impact performance is not unique for a given test. It dependends on the component locations. In addition, the corner component locations give worst drop impact performance. This has nothing to do with the reliability of the component itself. Rather, it is affected by mounting

screw. Including the corner components in JEDEC drop test evaluates the effect of mounting screws very close by, instead of assessing the intrinsic drop impact performance of the components itself. An improvement of JEDEC drop test would be excluding the corner components for drop impact performance relative comparison among packages.

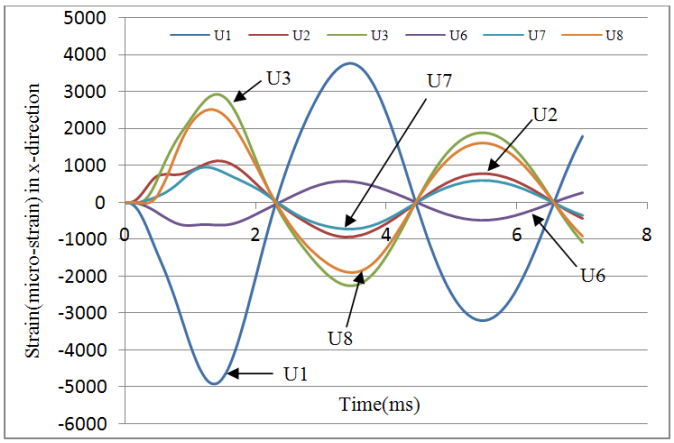


Figure 14. Comparison of board strain at chip corners

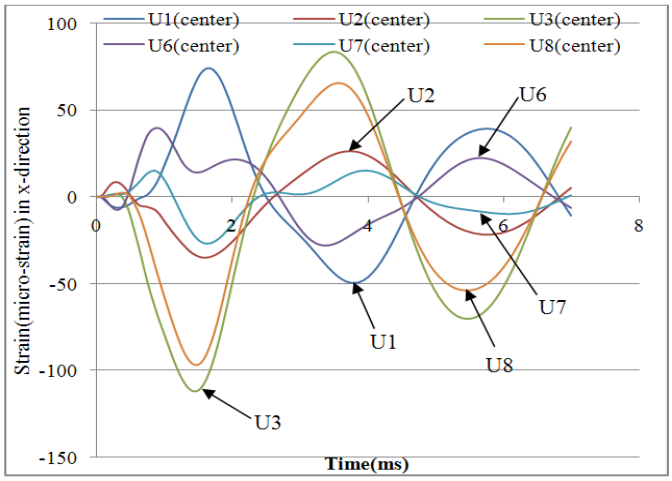


Figure 15. Comparison of board strain at the center of chips

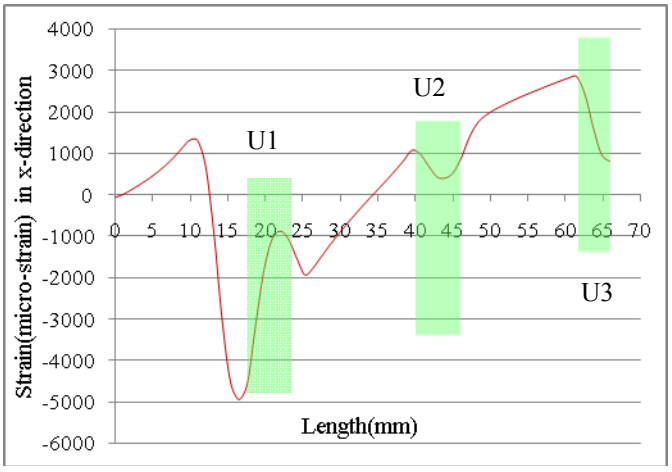


Figure 16. Board strain distribution at specific chip loactions

Figures 16 plots the board strain at t=1.5ms U1-U2-U3 paths, one through center of components and one is 1 mm away from component edges. It is shown that the board strain amplitued along the path 1 mm away from the component is in general higher the path through the center of the components. This is because the first path captures the maximum strain at component corners. It is also observed that at the center of the chip the strain is minimum due to board stiffening by the component. In figure 17 the shaded region in this figure is where the component is mounted. Again it is seen that the board strain beneath each chip has a 'U' shape pattern, which means that the center strain is the lowest. There is a very large strain gradient close to the package edge. This suggests that the strain gage placed in the center of compoenets on the PCB cannot reflec the board bending behavior, but will be good for the simulation validation. The strain gage at the package corner will be very sensitive to the location due to the large gradient shown in this figure. Between U1 and U2 the vending direction changes. And there is a stationary point (node). When a strain gage is attached in the middle of two component, it might not give useful information since it might be close to the node.

5.4 Effect of Acceleration on Board Strain Disribution

Board strain is studied for the effects of different loading cases of accelerations. Here input acceleration of 1000g, 1500g and 2000g are considered. The board strain history in x-direction at t=1.5ms is plotted in figure 17 for applied loads. It is shown that with increase in the G load the value of strain increases.

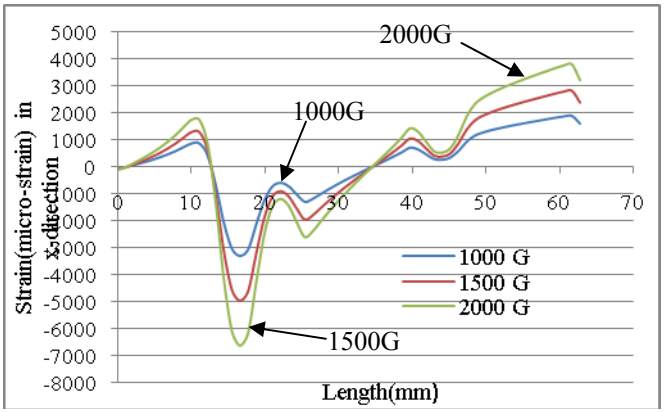


Figure17. Comparison of board strain for different values of acceleration load

5.5 Effect of Chip Size on Board Strain

The effect of chip size on the board strain is studied. The chip sizes 3x3, 4x4, 5x5, and 6x6 are taken into consideration to see how the chip size influences the board strain. The board strain is plotted in figure 18 for different chip sizes. It is seen that as the chip size increases the board strain in the chip region decreases. This is because large components stiffen the board more. The strain amplitude peak near component increases with chip size increase, while strain far away from the component location does not change with the size of the chip. Therefore, it is essential to place the strain gage close to the edge of the components to capture the variations. It can be seen that the board strain amplitude increase with chip size is

not significant. The detailed study on the effect of chip size on solder joint stress will be reported in the future.

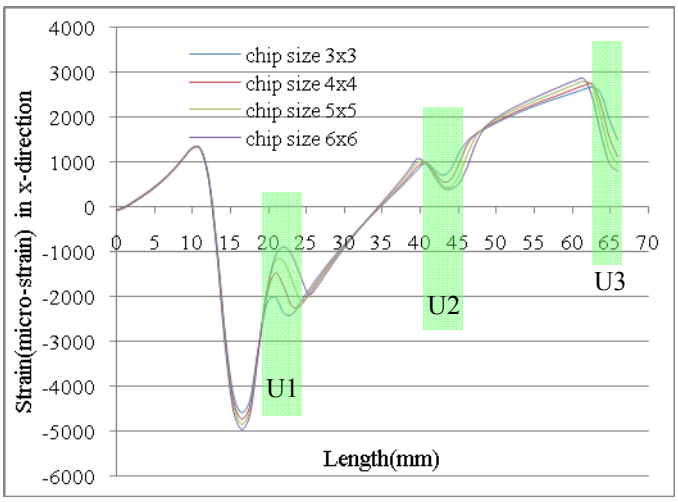


Figure18. Comparison of board strain for different chip sizes

5.6 Effect of Boundary Conditions for Direct Input Acceleration Method

In order to assess the effect of boundary conditions, two boundary conditions at mounting hole are considered. This first case incorporates displacemet components in x, y, and z directions for nodes at the mounting hole being fixed. The second case incorporates displacement in z-direction only is fixed for nodes at the mounting hole. The models with these two sets of bondary conditions are studied with input acceleration method. The board strain is plotted in figure 19. It is seen that slightly different results are obtained for the two different boundary conditions. The theoretical study on the model study will be reported in the future.

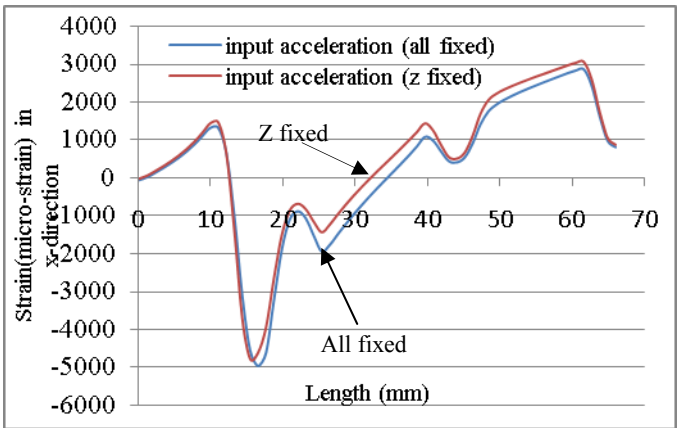


Figure 19. Comparison of board strain for different boundary conditions in input acceleration method.

6. Conclusions

Based on the studies in this paper, it is recommended that, in order to achieve the computational efficieny without the loss of accuracy, a solder layer model for wafer-level packages with direct acceleration input using full transient implicit anaysis provides an accurrate and fast board dynamic response analysis. The mode superposition in ANSYS does not have an advantage in saving computation time since the solution expansion process is needed. The input-G and direct acceleration methods give exactly same results with certain boundary conditions. Neither Input G or Dierect Acceleration Input method truly represents the actutal loading conditions during impact. A thereotrcial model study will be reported in the future.

Components near mounting holes may fail first during drop test. This failure rate has nothing to do with the package intrinsic drop impact performance, rather it is due to the effect of the mounting screw. An imporvement to JEDEC drop test procedure may be excluding the corner components when reporting the drop test performance of a package.

This paper focuses on the board global dynamice response analysis only. The solder joint stress analysis and its relationship with the board strain is not included in this paper due to space limitation. The detailed local modeling and solder joint stress analysis will be presented in a separate paper.

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